WHAT IS CLAIMED IS:

1. A system for accelerating ASIC design verification by eliminating clock skew and race conditions in a digital circuit design comprising;

a computer;

said computer having random access memory;

digital circuit design files being stored in said random access memory;

a design verification manager program for processing said digital circuit design files being stored in said memory, said design verification program including,

a find clock sources subroutine for finding clock sources in said digital circuit design file,

a find synchronous primitives in said digital circuit design file that are receiving clock signals from said clock sources found by said find clock sources subroutine,

an inserting edge detector circuits subroutine for inserting edge detector circuits between said clock sources found and said synchronous primitives;

whereby the verification of digital circuit designs is accelerated.

2. The system according to Claim 1 wherein said design verification manager includes; a subroutine for finding and

replacing synchronous primitives without a clock enable input with synchronous primitives having clock enable inputs.

3. The system according to Claim 1 wherein said design verification manager includes a subroutine for analyzing connections between inputs to said synchronous primitives and outputs from said synchronous primitives and inserting a data buffer between said inputs to said synchronous primitives and output from said synchronous primitives.

4. A system according to Claim 1 wherein said design verification manager includes a find falling-edge clocked primitives activated with a falling clock-edge and substitutes rising clock-edge primitives for said falling clock-edge primitives.

5. The system according to Claim 1 wherein said design verification manager includes a subroutine for finding rising edge clocked primitives activated by a rising clock-edge and substitutes rising clock-edge primitives with falling clock-edge primitives.

6. A system for simulating digital circuit designs comprising;

a computer;

said computer including memory for storing design files;

a design verification manager program for processing said

design files stored in said memory;

a simulator program for simulating design files or a selected part thereof stored in said memory;

test bench files for stimulating operations of said simulator;

said computer including a hardware accelerator;

said design verification manager program including a subroutine for splitting a design file into a selected simulation file and a selected hardware execution file;

said design verification manager program downloading said selected simulation file into said simulator and downloading said selected hardware execution file into said hardware accelerator;

a subroutine in said design verification manager program for finding clock sources in said selected hardware execution file;

a subroutine for finding synchronous primitives with clock-driven inputs in said circuit design file that are receiving clock signals from clock sources;

a software subroutine for inserting edge detector circuits between said clock sources and said synchronous primitives;

said find clock sources subroutine, find synchronous primitives subroutine, and said inserting edge detector circuit subroutine operating on said selected hardware execution file by said design verification manager;

whereby digital circuit designs verification may be accelerated.

7. A system for simulating digital circuits according to Claim 6 wherein,

said hardware accelerator includes,

target hardware,

a temporary buffer,

a driver buffer,

said simulator includes,

a subroutine for performing functional simulation of said selected simulation file,

a subroutine for detecting the end of simulation of selected

simulation file by said subroutine for performing functional simulation,

said hardware accelerator including;

a subroutine for transferring data to said temporary buffer,

a subroutine for detecting the end of data transfer to said temporary buffer,

a subroutine responding to said subroutine for detecting the end of data transfer to said temporary buffer and causing data transfer from said temporary buffer to said driver buffer,

and

outputs of said driver buffer being applied approximately at the same time to said target hardware input signal lines.

8. A system for simulating digital circuits according to Claim 7 wherein,

said hardware includes,

an input signal buffer,

said simulator includes,

a read input signal buffer subroutine for reading data from a hardware accelerator into said simulator,

said input signal buffer storing inputs from logic elements within said target hardware,

a hardware timeout subroutine,

said hardware timeout subroutine being responsive to said subroutine for responding to the detection of an end of data transfer of and causing a read data from said input signal buffer to simulator wherein reading of said data takes place at a time that is determined preferably in terms of simulator internal clock, said time being in duration from one to one hundreth of said simulator internal clocks.

9. A system for simulating digital circuits according to Claim 7, wherein,

said hardware accelerator includes a read detector circuit,

an input signal buffer,

said simulator includes,

an interrupt subroutine,

a read input signal buffer subroutine for reading data from input signal buffer into said simulator;

said input signal buffer storing output from logic elements within said target hardware;

said read detector circuit being responsive to signal processing within target hardware and producing an interrupt signal upon completion of said signal processing;

and

said interrupt subroutine being responsive to said interrupt signal and causing reading of data from said input signal buffer to said simulator wherein the reading of said data is preferably instantaneous.